Concurrent Divide-and-Conquer Library with Petascale Electromagnetics Applications

Johan Carlsson, Tech-X Corporation

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### Implementation of Bowers implicit field update in VORPAL

Tue 10 Feb 12:25:05 Added the proper expressions for the coefficient-matrix elements (including Bowers' damping coefficient, etc.). Tue 10 Feb 19:56:03 This afternoon's changes. Wed 11 Feb 15:46:34 Coded up the right-hand side. Wed 11 Feb 18:53:23 The core code should now be pretty much complete (setting up coefficient matrix and RHS, updating the field). Thu 12 Feb 19:13:53 The code now builds. Mon 16 Feb 18:26:35 Bugfix. Now it builds with HAVE\_AZTEC defined. Fri 20 Feb 11:18:07 Misc bugfixes. Tue 24 Feb 21:49:24 Minor changes, still having convergence сн problems with the iterative solver. Wed 25 Feb 19:44:23 Several critical bugfixes! Implicit solver now seems to work. Johan Carlsson Concurrent Divide-and-Conquer Library

# Performance of Bowers implicit field update in VORPAL







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#### **Concurrent Divide-and-Conquer**

• Keep multiple tridiagonal solves in flight simultaneously to overlap communication with computation



### Scalability formula can be derived

- Let  $C_{1D}$  be number of cells in one direction, so that  $C_{3D} = C_{1D}^3$
- Let  $N_{1D}$  be number of processors in one direction, so that  $N_{3D} = N_{1D}^3$
- Let  $\tau_{cell}$  = time it takes to do backsolve of a single cell
- Let \(\tau\_{latency}\) = time it takes to receive a message
- Then the maximum number of cell-rows that can be done simultaneously by a processor is  $N_{cellrows} = C_{1D}^2/N_{1D}^2$
- A processors share of the common-matrix-inversions is therefore, *N<sub>immediate</sub>* = *N<sub>cellrows</sub>*/*N*<sub>1D</sub>
- The number of cells in a single-processor's backsolve is  $N_{cellsSolved} = C_{1D}/N_{1D}$

So immediately following a processor's common-matrix-inversion-and-send on the  $N_{immediate}$  matrices, it can proceed with  $N_{immediate}$  backsolves, which will take a time:

#### $N_{immediate}N_{cellsSolved}\tau_{cell}$

to perform. This must exceed  $\tau_{latency}$  in order to ensure that there is no idle processor time.

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# Might be possible to achieve good scaling on biggest available machines



